DON McARTHUR & JEFF SCHIER

Digital Image Processor, 1976

THERE ARE AT LEAST TWO OF THEM in one body, Jeffy and Jeff. Jeffy of course is playful, funny and fast. Jeff is a reincarnated police interrogator. They both live with a third person, Diane in a little wooden house erected right over a long forgotten geological fault in Oakland.

Without him, being our student in Buffalo, we could never have gotten our education. Luckily, the only way Jeffy, living in the left hemisphere could inform Jeff living in the other, was through the acoustic interface of speech. To close the circuit, an interlocutor had to be found, Steina or me. That's how we learned.

Jeffy vastly expanded the McArthur concept. He put several modules on the bus, elevating it from mathematics to a visual experience. But his true masterpiece, "The Image Articulator," was yet to come.

—W.V.

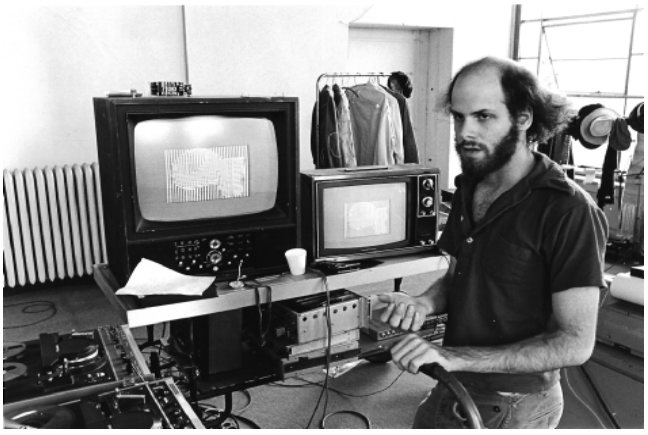
JEFFREY SCHIER was educated at the State University of N.Y. in Buffalo, where he worked as a design engineer for the Vasulkas. During that time he facilitated the software/hardware interface of several unique video processing machines to a DEC LSI-11 microcomputer: George Brown Multi-level Keyer, Seigel Colorizer, Rutt/Etra Scan processor. Schier was the co-designer of the MacArthur/Schier real-time Image Processor. Later he designed and implemented the Image Articulator: a bit-slice frame buffer with real time image manipulation abilities. Subsequently, he worked as project leader for color graphics CAD Workstation applied to PC board design; he was lead designer of the GMR2800 Computer Graphics Image Processing system at Grinell Systems, and he has worked as a senior research engineer at Cubicomp Corporation, and at Aurora Systems. From 1987-89 he worked for Pinnacle Systems as project manager for development of PriZm digital video effects system (DVE). The DVE performs real-time rotation, perspective transformations, and curved/warping of the image; with the aid of a color menu interface. Presently, he works at Chips and Technologies, Inc. as Staff Design Engineer.


FRAME 225

DIGITAL IMAGE PROCESSOR

The Schier/McArthur Digital Image Processor was constructed in 1976-1977 at Steina and Woody Vasulka's loft in Buffalo, N.Y. It began as a mathematical exploration by Don McArthur of the digital raster and was built from digital modules locked to video time by a 16 bit micro-computer: a DEC LSI-11. It was built in stages starting with the sync generator and computer interface. A digital Selector, Arithmetic-Logic Unit, lookup/pattern RAM and a rectangular Window Generator were added later. The video outputs came from three 4 bit digital to analog converters, and was converted to color composite video by an external NTSC color encoder. The video tape recorder was on continuous standby, allowing documentation of the design process by Steina through "pressing the record button."

The modules were "wire-wrapped" and connected to the computer control and timing bus at the rear of the modules. The digital video paths were patched together with multi-conductor ribbon cables plugged into the front of each module. External audio could be patched in or out from the front panel, converting the video timing signals to sound. Emphasis was placed on internal square waveforms to form the first pictures made from the horizontal and vertical bar patterns that subdivide the raster. A borrowed time base corrector was "hot-wired" to pull out 6 bits of live digital video from its A to D (analog to digital) converter and color-mapped through the lookup/pattern RAM. A random "power-up" pattern was saved from the RAM and formed a favorite color test pallette for adding colors to the image. The real-time



Left: Jeff Schier in the Vasulkas loft, 1977, Buffalo, New York. Photo: Woody Vasulka.
Below: Digital Image Processor.

remapping of intensity to color formed a color precision (64 levels) unseen in analog colorizers. Dual four bit Analog to Digital converters were later constructed to digitally combine two image sources. Operations were performed at 4 bit resolution per red, green and blue channel, but were funneled down to 6 bits when running through the lookup/pattern RAM.

The digital combination of binary images formed unique geometric color patterns. These were unexpected and did not correspond to other analog processes. This became evident when the Arithmetic/Logic Units (ALU's) were installed. The ALU's performed arithmetic functions (addition, subtraction), and logical functions (And, Or, Exor, Negation) and wacky mixed arithmetic and logical operations that were "thrown in" by the semiconductor vendor, such as (A OR B plus 1). The bitwise combination of image combined with overflow/wrap-around conditions generated unusual patterns of color and box-like textures without equivalence in analog video. The binary operations made sense but the images were a digital surprise. "Official" test images were needed to test out the ALU process. This consisted of a white styrofoam sphere or cone and Woody's hand waved in front of the camera. These test images contain 16 discernible levels of grey, useful to disclose the arithmetic/logical binary combinations and overflow conditions. The explorations of real-time digital video at the Vasulkas predated later image processing and digital video effects units. The exploration of binary operations between images has largely been ignored

in image processing and computer graphics in it's quest for photo-realistic imagery.

Time-locked software marching to the video frame rate formed the real-time control structure needed to operate the digital image processor. Various test and control table programs were written in Fortran and PDP-11 Assembly language to operate the processing modules. Walter Wright programmed "BARBAR," an assembly language control program with independent timing control stacks. BarBar's timing stacks control processing module functions, time delays, and the looping of the control sequence. The inclusion of random functions exercise the hardware, contributing to long sequences of digital permutations.

The hardware consists of a rack of digital processing modules, a gen-locked sync generator, a vertical interval control bus, and a microcomputer to orchestrate the field by field control. The digital video paths for the processing modules are "patched"

through their front panels. Signal Path: Input is received through camera sources, video tape sources, or the internal pattern source (H and V timed bar patterns). The camera and VTR sources route through the A/D converters first. There they are front panel patched to the processing modules and converted back through the D/A converters into RGB video and then to a RGB to NTSC encoder for composite color output.

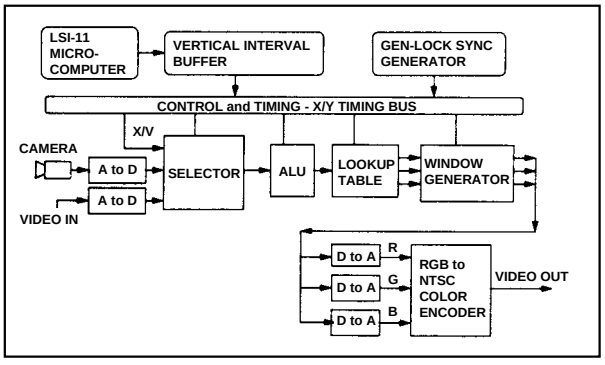
1) Microcomputer: a 16 bit DEC LSI-11 microprocessor coordinates control words for the processing modules and handles user interface functions.

2) A Vertical Interval Control Buffer and Transfer Bus: control information is loaded into this control buffer by the microprocessor during the current active field. The data is shipped down to processing modules during the next vertical blanking interval.

3) Processing Modules:

A) Analog to Digital Converters (A/D) consisting of two 4 bit converters.

B) Selectors (3 groups) which choose between 8 horizontal, and 8 vertical frame-locked patterns, and an external digital source. The selectors allow bit-wise selection of horizontal/vertical timing components and external video inputs.



C) Arithmetic Logic Units (ALU's) which combine two digital input streams into a single output through combinations of arithmetic and Boolean logic functions (Output = function (A_in, B_in). The Boolean functions of 'AND,' 'OR,' 'EXOR,' 'EXNOR,' Ones Complement are present. The arithmetic 'A PLUS B PLUS CARRY,' 'A MINUS B PLUS CARRY,' 2's Complement are also available. Certain combinations of arithmetic with logical operations are possible, with a 'Constant' available on the 'B' input, useful for bit-masking.

D) Lookup consisting of an RGB lookup table with common digital address input is present to perform intensity/pseudo-color transformations. The memory could be loaded then scanned out as a small raster.

E) Window generator: three Window generators form an adjustable frame for gating/routing the digital sources. The frames are independently programmable on a pixel/line basis. Wipe patterns and title boundaries are formed by the same principle.

F) Digital to Analog Converters: one apiece for Red, Green and Blue components at 4 bits per gun.

4) A Gen-Lockable Sync Generator which forms sync timing, and subdivides the active screen into 512 H by 486 V coordinates. Both video sync and H and V timing information is available on the control bus to be picked-off the modules' program. A Phase Locked Loop locks the clock timing to an external sync source.

5) RGB to NTSC Color Encoder comprises the funnel for output and converts the RGB signals from the D/A converters to an NTSC color composite video signal for display and recording onto video tape. —J.S.


INFO frame 46627 to 50399


NANO B frame 42995 to 49989