A DEscription of the Voltage to Position Converter a portion of the Direct Video Synthesizer, A Real Time Electronic System for Generating Color Graphics in the Television Format

Stephen C. Beck
May 29, 1971
EE 199 Individual Study
Berkeley, California

Contents of Discussion

Introduction

In the search for a more precise method of controlling light as an expresive tool I was attracted to the potentials of video. I began working with what is now called Direct Video while attending the University of Illinois at Urbana, in the fall of 1969. Other image generating techniques, computer graphics for example, were intriguing, but access to the machine was limited, and most systems required a great deal of hardware. It seemed to me that a more efficient method of generating graphics in real time could be developed around hybrid circuits which would actually produce image parameters under the direction of a controlling computer.

Since September of 1970 I have been developing such circuitry under a National Endowment for the Arts fellowship at the National Center for Experiments in Television, at KQED in San Francisco. I have been able to prototype a modest array of circuitry for producing camera-less images on video display monitors. The approach is as general as possible so as to maximize the posibilities for image production while minimizing the actual hardware involved.

Without elaborating in great detail the entire system design let me define four parameter classes which are applied to form the basis of the image generating circuitry:

1) Geometry, which includes the 'order of the geometry', either points, lines, or planes; definition of contours and regions; establishment of perspective cues for three dimensional illusions;

2) Motion, where the display surface is considered to be a catesian plane and the elements of geometry may translate or rotate with respect to the reference system of the scan; the rate of translation or rotation;

3) Texture, that is, local and temporal variations over an arbitrarily defined region about some point in the image field;

4) Color, which is the hue, saturation, and brightness of texturized geometry;

Different modules of voltage- controlled circuits serve to control these parameters. Figure 1 is a block diagram of the system as it is envisioned at this time. To maintain generality,the image generating portion of the system is independent from the particular video format chosen. I am working with the American NTSC format but there is no reason that the techniques could not be applied to other video format, Phase Alternating Line (PAL), SECAM, or high resolution, to cite a few, since the encoder makes the necessary adaptations.

In the experimental setup a Telemation broadcast synchronizing generator is the master clock, supplying stable horizontal and vertical pulses and the chrominance subcarrier. A 3-M brand encoder forms the composite video signal from information leaving the color section of the image generator. The output of the encoder is a standard NTSC color video signal which meets all FCC timing requirements. This signal may then be displayed on a color television monitor, recorded on video tape, or used to modulate an RF carrier.

For the rest of this description I will be discussing the geometry section, particularly the voltage to position converters, the reference signal generators, the geometry logic array, and a contour voltage source.

The Voltage to Position Conversion Scheme

The video display format consists of a series of vertically stacked horizontal lines which represent the locus of the electron beam as it scans the cathode ray tube. The scan begins at the top left corner of the display surface and procedes, in the same manner as we read a page of print, from left to right, across each line sequentially from top to bottom of the raster. The total lines contained in one complete scan number 525, of about 28 of which are not visible and are reserved for the retrace of the scan from the bottom of the raster to the top, constituting the vertical interval. Similarly, a portion of each line is reserved for retrace from the right to the left side of the raster. On any given pass of the scan from top to bottom every other line is scanned, which comprises a field. On the succeding pass the alternate lines are scanned completing a second field and one complete frame. The period of each frame is approximately 33.33 milliseconds while the total usable time in each line is 52.5 usec (microseconds).

In its simplest form the voltage to position conversion scheme consists of arithmatically comparing a reference voltage, which is an analog for the position of the scan, and a position defining control voltage, and on the basis of the comparison determining when the electron beam should be gated on. Figure 2a depicts the voltage waveforms involved in a comparison and the associated image which is generated. The reference voltage is a linear ramp waveform which is synchronized to the scanning rate and bears a constant phase relationship to it. The control voltage is set with a potentiometer. Figure 2b shows the image generated when the reference signal is at the horizontal rate, T= 52.5 usec, while figure 2c shows the result with a vertical synchronizing, T= 16.67 msec.

With the simple circuit described a unique position is defined on the display surface as the point represented by the intersection of the two edges. At the same time there is plenty of information generated in the comparison process to produce points, lines, and planes which are defined by two control voltages, E_v in the vertical dimension (y- axis) and E_h in the horizontal dimension (x- axis).

Use of the ramp waveform as a reference signal produces what is called edge- reference symmetries as a sweep through the control voltage range moves the addressed coordinate from one edge of the raster to the other. When both E_v and E_h are zero the addressed point lies at the center of the raster which becomes the origin. Due to the 3:4 aspect ratio (vertical size:horizontal size of display surface) use of reference voltages for both the H and V directions which are the the same amplitude produces a catesian plane with a 3:4 aspect ratio. This is simply a matter of scaling and can be varied by selecting different amplitudes for the reference voltage.

Consider the displayed image with a different waveform for the reference voltage. Figure 2d depicts the use of a triangle waveform to obtain center symmetry where a sweep of the control voltage moves the edge toward or away from the center of the display. Various waveforms may be used as reference signal, not necessarily linear voltages but always synchronized to the scan rate.

Realization of a reference generator which produces both ramp and triangle waveforms synchronized to the vertical and horizontal scan is shown schematically in Figure 3.

As seen from the basic schematic the ramp voltage is generated by charging timing capacitor C with a constant current and then discharging C during the blanking interval. Refering to the schematic, Q3 is the constant current source with value set by R1. Diode D1 is thermally coupled to Q3 and serves to track the reference voltage with changing base-emitter characteristics over temperature variations. Q2 acts as a saturated switch which clamps the voltage on C to a value set by R2, nominally -2 volts. Q2 is driven by level shifter Q1 which accpets the negative going blanking pulses from the sync generator, at either the horizontal or vertical rate. (the circuit shown is actually built twice, one for each rate). Commutating capacitors on the base resistors of Q1 and Q2 serve to speed up the discharge of C so as to achieve a stable state as quickly as possible. C2, D2, and logic inverter I1 provide RTL logic level blanking pulses for logic in the rest of the system.

The waveform at C is 4 volts peakto peak with a bias level of zero volts. The relationship

$$\frac{I}{C} = \frac{\Delta V}{\Delta T}$$

determines component values, where I is the value of the constant current source, C the timing capacitor, ΔV the desired waveform amplitude, and ΔT the period. A bipolar voltage was chosen so as to obtain maximum range of operation of the comparators in the voltage to position converter; within their common mode range. Operational amplifier A1 is a follower which does not appreciably load C as its input bias current is about 2 orders of magnitude less than the constant current source charging C. Complementary current boosters Q4 and Q5 provide a very low output impedance which will drive several comparators independently. The low source impedance reduces errors at the comparator by minimizing voltage offsets produced by the input bias currents of the comparator.

Further processing of the full-wave rectifier and level shifter A2 and A3 producesthe triangle waveform. Q6 and Q7 provide low ouput impedance.

The operation of the rectifier is interesting: On negative portions of the ramp voltage D4 conducts and the voltage at point a is -V/2 where V is the peak to peak value mentioned earlier. A3 performs the operation $-2(+V/2)-4(-V/2)= V$. On positive portions of the input ramp D3 bounds A2 and D4 causes point a to be zero volts so the output of A3 is $-2 (V/2)=-V$. The result is a triangle waveform with peak to peak voltage of 4 volts with a bias of -2 volts. R3 removes the bias while the external 20 kohm resistor allows the bias to be varied with an external voltage.

The circuit showm here has been prototyped on a Vero circuit card and operates excellently. The waveform linearities are better than 1% accurate and display good temperature tracking, the amplitude varying only .1 volt over a four hour period from cold start, an error of 2.5%. This error can be reduced by redesigning the current sources using dual montlithic transistors rather than heatsinking an diode to a transistor. The generator output impedance is on the order of 10 ohms.

Extension of the Conversion Scheme.

The information contained in the pulse outputs of the comparators can be processed in a variety of ways so as to produce planes, lines, and points in the display. Figure 4 depicts such a system. (The switches shown are actually digitally driven FET or logic gate switches which are operated during the vertical interval (approximately 1.2 millisec in duration) so that changes in the processor state are not visible in the displayed image.) Reference also to figure 6 will aid in visualizing the different configurations produced by the processor.

In Figure 6a the reference select switches are in the edge reference position , the reference waveform is a ramp. Row i shows the outputs of the inverter buffers of the voltage to position converters, Q and $\underline{Q}$ for both the H and V dimensions. Switches A and B are each in the planes position. The output signals form the gates of the logic array drive the electron beam in the display tube by modulating the amplitude of the Y component of the video signal (the luminance component, white level) and the amplitude and phase of the chrominance subcarrier (the color hue and saturation of the image). The displayed images are depicted in rows ii and iii

of figure 6a for various configurations of Qand Q. Simultaneous output signals which are complements of one another allow for independent modulation of the regions.

Horizontal and vertical lines may be produced by triggering the monostable multivibrators which comprise the geometric unit generator. Figure 5 depicts the schematic of the monstables. A monostable multivibrator is formed by gates G1 and G2, and Ct and R1 in series with 1 kohm. G3 and G4 buffer the monostable output pulse and provide complementary pulse outputs. G1 is triggered by a positive edge. In the case of regions which have both a leading and a trailing edge within the period of a line the monostable must be triggered on both the positive and negative edge; to perform this operation, which amounts to taking the absolute value of the differentiated input pulse, a pre-trigger processor is utilized. The 220 pf capacitor differentiates the input pulse, the differentiated signal being steered to either Q1 for positive pulses or Q2 for negative pulses, with positive pulses generated at the emitter of Q2. The monostable period may be varied over a range of .5 usec to 20 usec or from 60 usec to 250 usec, for producing vertical and horizontal lines respectively. The horizontal lines consist of from one to four scan lines (actually twice that number due to interlace), while the vertical lines can be varied from very fine width (1 % of the raster width) to very broad, all variation achived by changing potentiometer R1 and by switching the value of Ct.

Figure 6a row iv shows the image display of processed line signals. At last the one point which is uniquely defined by the two position control voltages is visible ! Figure 6b demonstrates the same processing for a center reference pattern. Line and point generation may also occur after the logic array, in which case arbitrary regions may be outlined. There is a problem in outlining which is discussed later in the description.

Up to this point the development of the processor proceeded as anticipated. I originally thought that the position determined by the two control voltages could be used simply as an address on the display for locating an arbitrary shape which would be generated by some other circuitry. However,

Some Present Limitations

Despite the flexibilty that the system allows for translating planes, the ability to rotate and to create the illusion of revolving in space is not easily obtainable. Perspective cues may easily be established which allow for translation in an illusory three-space but rotation about an arbitrary origin cannot be obtained. However, I am confident that this problem can be solved by generating an appropriate reference voltage. The beauty of the reference signal method is that an image may be established and, despite the number of independent portions of the image, by changing the reference signal the whole image field is mapped accordingly into a different location.

I cannot describe the reference signal for rotation although it will undoubtably be some form of phase modulated ramp voltage. Should I be incorrect in assuming so simple a solution, a solid state memory with read-write capabilities could be utilized to store information about locations which could be read out to produce rotation.

One other problem that has already arisen is the problem of outlining an arbitrary region. A vertical line is produced by a pulse only a few usec in duration triggered every 62.5 usec, while a horizontal line consists of at least one pulse 5usec to 50 usec in duration. As the slope of the line approaches zero the pulse duration must increase, the value being dependent on the finite separation of the actual scan lines and the desired slope. I am working on a voltage controlled monostable multivibrator which will allow a voltage to vary the pulse width from .5 to 500 usec. With such a circuit a correction voltage may be added to the basic width determining voltage so as to compensate for the varying slope.

Conclusions

With a relatively small amount of hardware the present experimental setup produces a wide variety of images. The economic demands of broadcast television have created a powerful technology for dealing with video images and it appears that the future development of cable distribution will

enhance televsion as a mode of communication for various sorts of information, not just the trash that appears on most commercial television these days. It stands to reason that image generating systems designed with the video format in mind will enjoy applications in the future, if not at the present.

To return to the controller, whether it be a person operating the parameters directly through mannual controls or by digital computer, or an interaction of the two, the ability to rapidly and easily change the controlling parameters is essential for obtaining the full benefits of the hardware. Aside from my interest in the art of technology in this project are aesthetic interests in the expressive and artistic use of the images produced. It is clear that in a medium which exists only in time the ability to precisely change the image is of the up-most importance. Eventually I would like to have an extensive digital hardware system for controlling the image parameters as well as a good software system and transducers for interacting with the controller. With this goal in mind I have been pursuing the voltage control scheme with the intent of first constructing a shift register sequencer with many cells, each cell containing several voltage storage elements, either potentiometers of digital storage with D/A and A/D capabilities. Eventually a small computer, perhaps a PDP-8 or whatever "they" have by then, would drive the voltage ports through D/A converters.

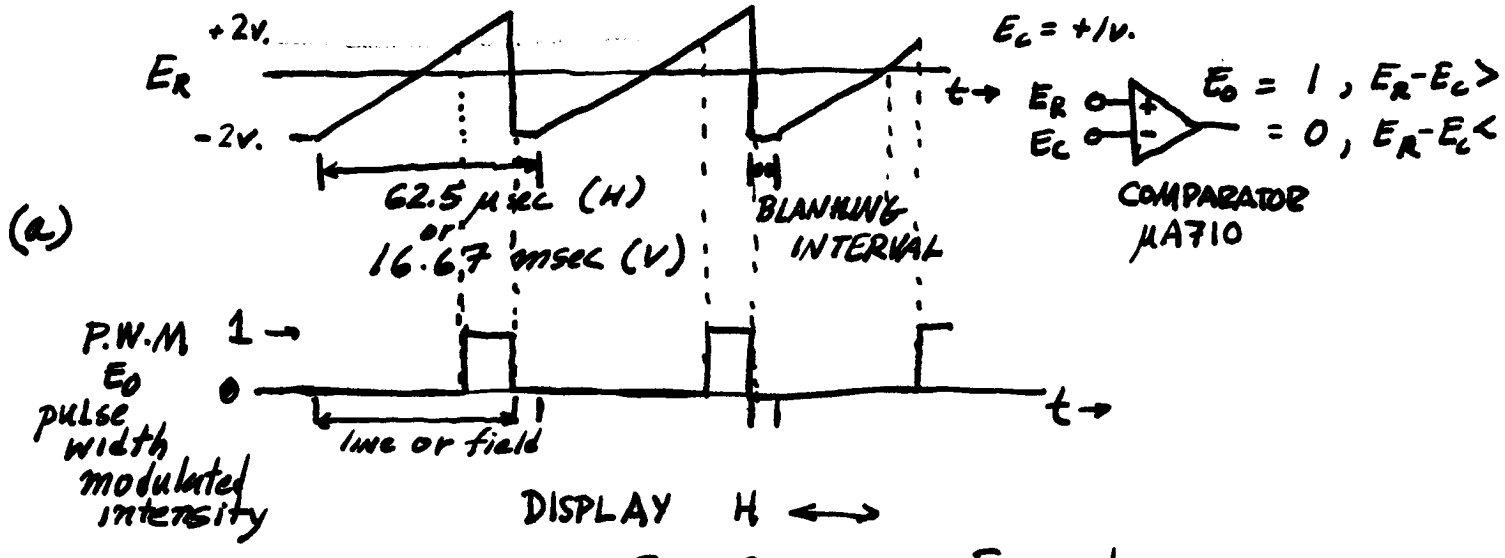
All told, this projects continues to be of great stimulation and excitement to me both technologically and aesthetically. As it gets more together more people might be able to experience the images, which puts a responsibilty on the person generating them. It is to this problem which I shall be directing myself in the next paper about Direct Video.

A good deal of the material written here I am considering to be proprietary while a patent search is being made. Please treat it accordingly.

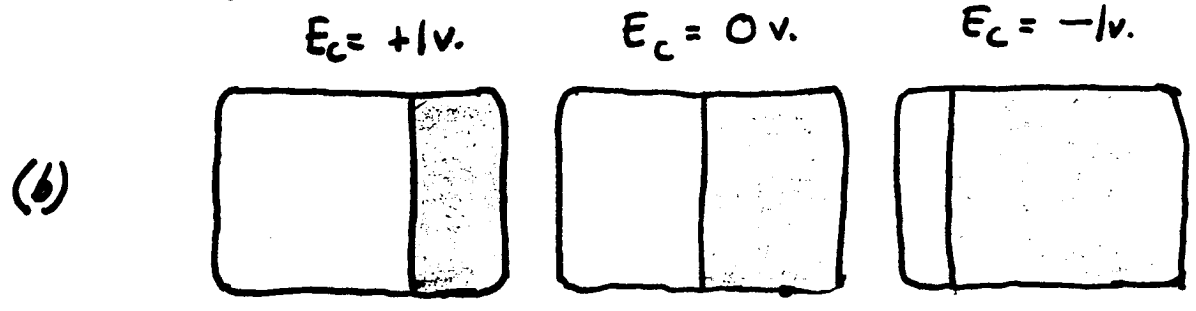
Stephen Beck

VOLTAGE TO POSITION CONVERSION SCHEME : FIGURE 2

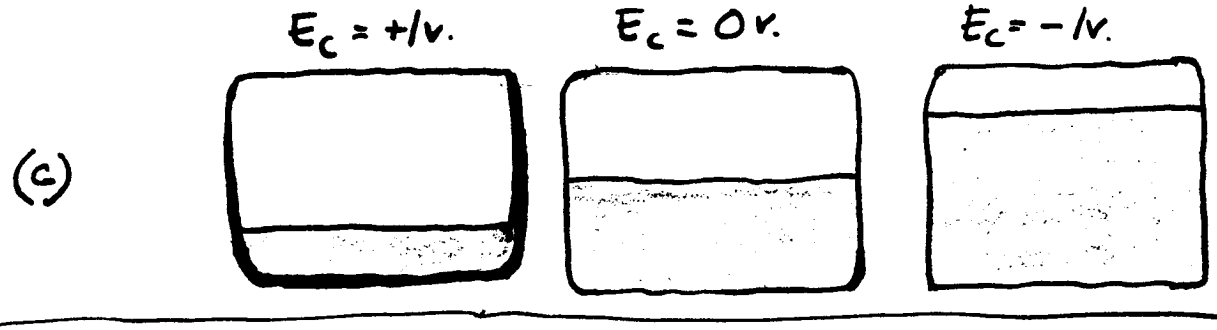
LINEAR TIME ANALOG REFERENCE VOLTAGE : EDGE REFERENCE



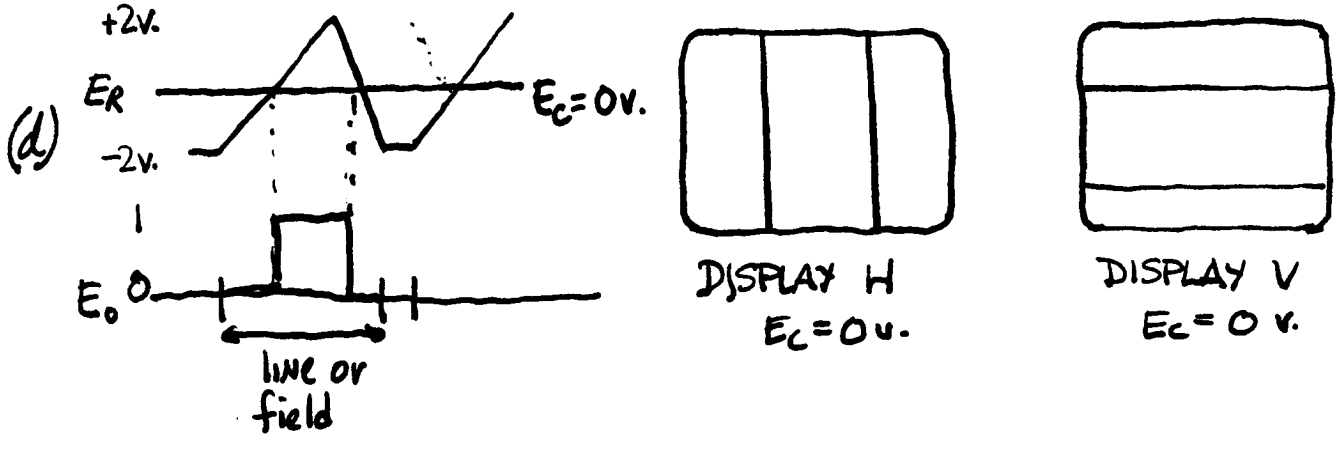
DISPLAY H ↔



DISPLAY V ↕



TRIANGLE ANALOG REFERENCE : CENTER REFERENCE



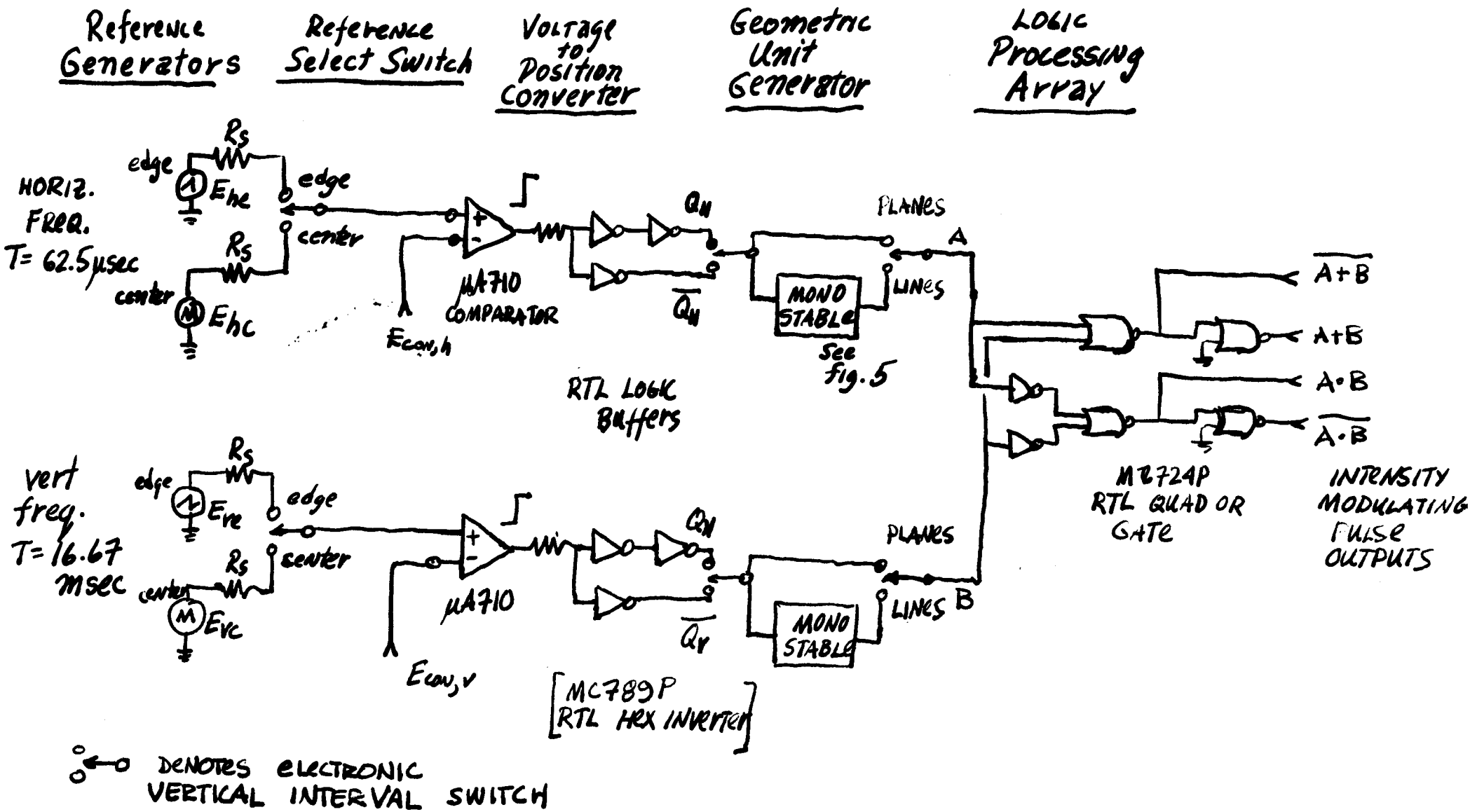
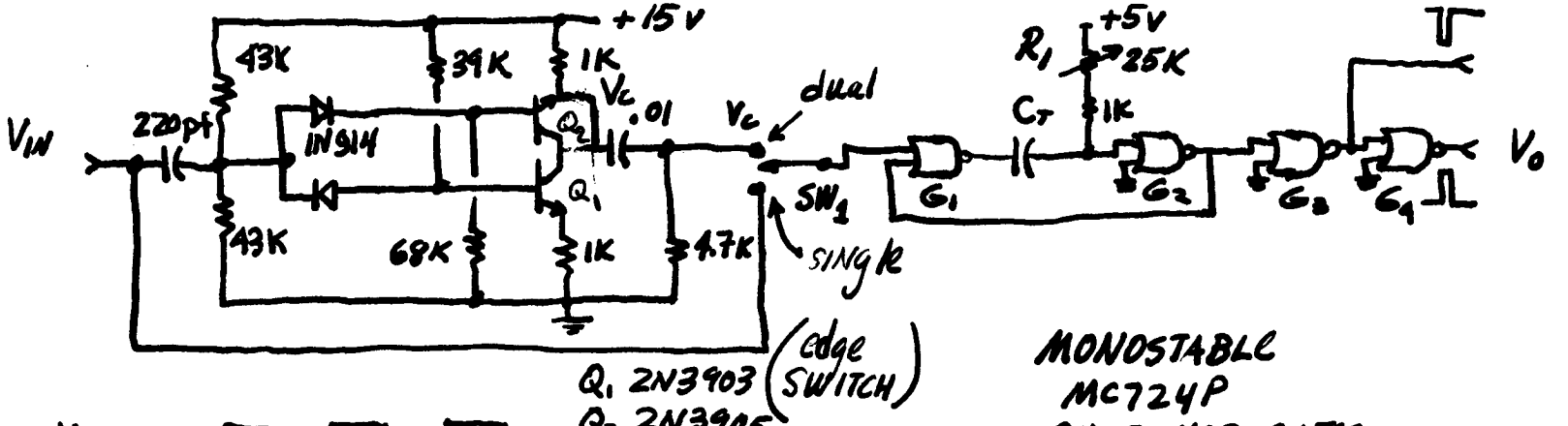


FIGURE 4 : SYSTEM BLOCK DIAGRAM : VOLTAGE TO POSITION CONVERTER

Geometric unit generator



MONOSTABLE
MC724P
QUAD NOR GATES
C_T = SWITCHED for T = .5μsec → 20μsec
or T = 65μsec → 250μsec

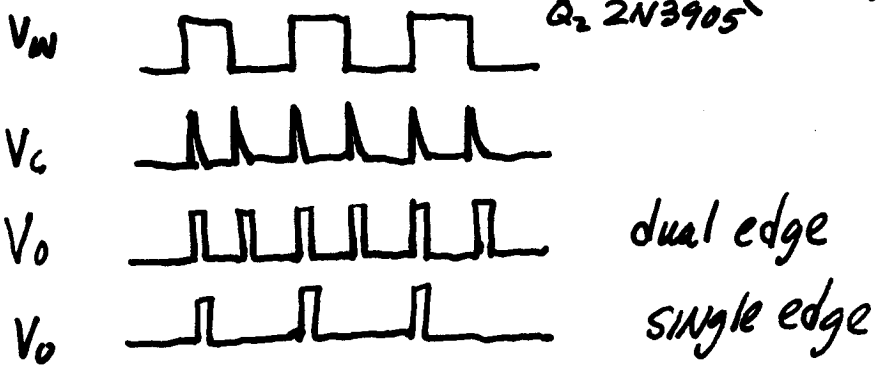


FIGURE 5 : MONOSTABLE LOGIC

FIG. 6: LOGIC ARRAY PROCESSING · RECTILINEAR REGIONS

(a)

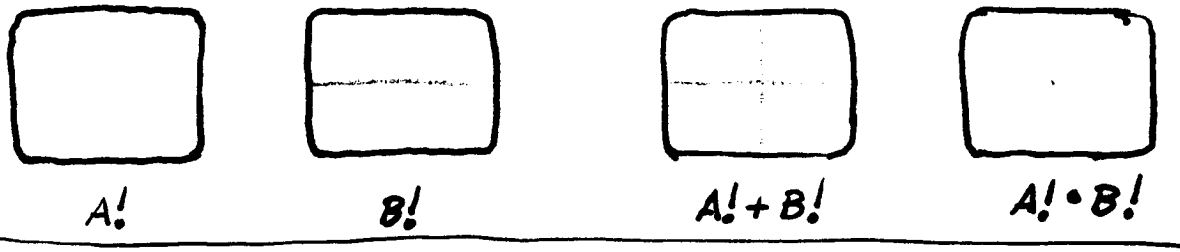
(i) edge reference $E_c = 0$ VOLTS

(ii)

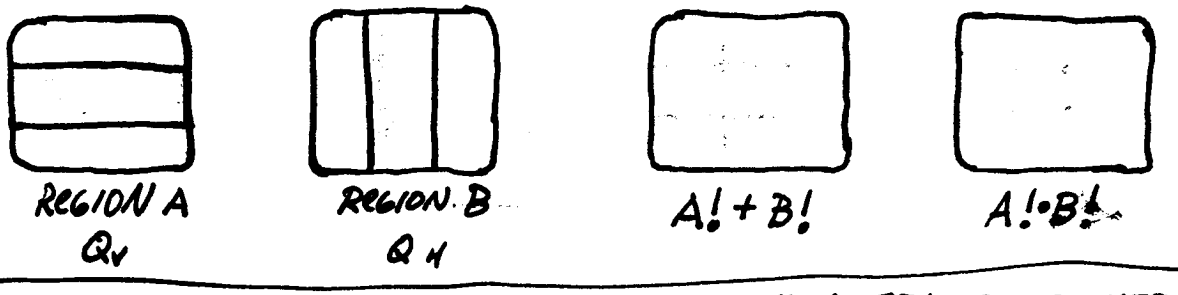
(iii)

LINE AND POINTS

(iv)

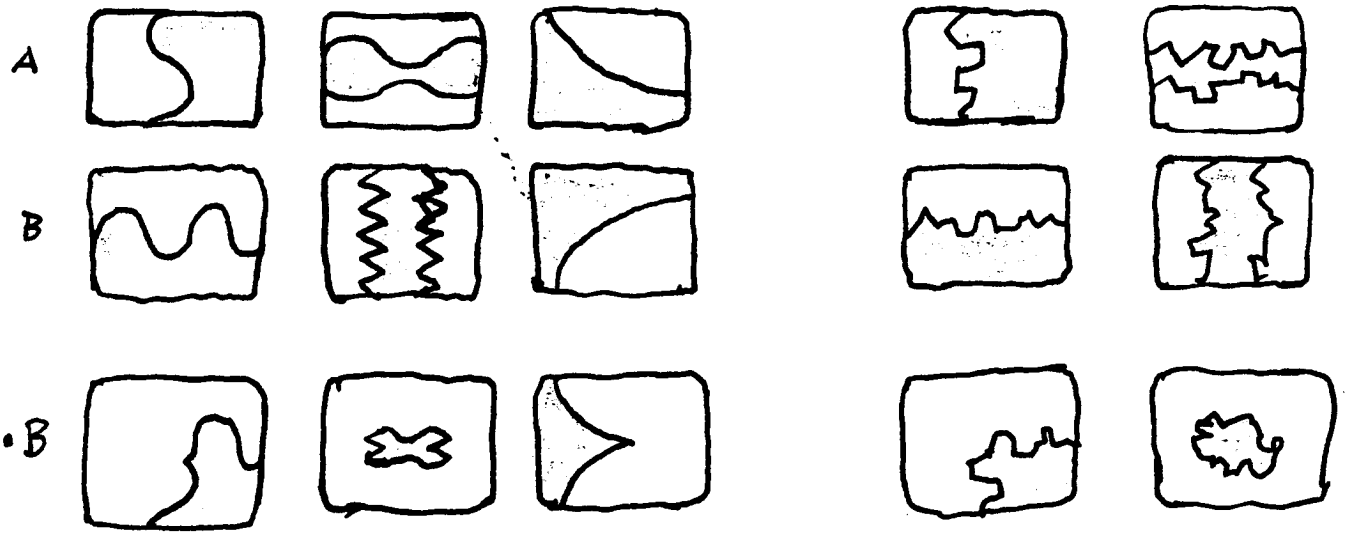


(b) center reference $E_c = 0$ v



(c) CONTOUR PROCESSING - NON-STATIC CONTROL VOLTAGE

SIMPLE regions COMPLEX Regions



5-71 SCB