THE UNIVERSITY OF MICHIGAN
MICHIGAN SOCIETY OF FELLOWS
Rackham Building
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Richard Mandeberg

GEN LOCK AND CAMERA INPUT

This module locks its output pulses to an external black and white, or color video signal inputted at JI1. In addition, the signal at JI1 is clamped, sync suppressed, and available at JO1 - JO4. This latter process is identical to one third of the INPUT module, except that the clamp signal is generated internally (consult IP documentation for explanation).

JO5 - JO14 are various synchronization and drive pulses at -4 volts into 75 ohms.

JO19 - JO22 are video signal outputs from cameras connected to the EIA-J 6 pin connectors.

The front panel LED indicates when the gen-lock is locked to an external source. Light ON means that lock is present, light OFF means the module is not locked. Outputted sync is only stable for recording when the light is ON.

CIRCUIT DESCRIPTION

Video at JI1 goes to the Sync Lock board which contains a TBA920 integrated circuit. The TBA920 is a combination sync strip and horizontal phase locked loop oscillator. Stripped sync is converted to proper TTL digital voltage levels by one half of the 319 comparator. Sync is also filtered to pick off vertical. This resultant vertical trigger pulse is buffered by the other half of the 319, and used to initiate the vertical timing process on the digital board. The horizontal oscillator locks in both phase and frequency to an external video source. R1 controls the free running frequency (no video input) of the horizontal oscillator. R2 controls the phase of the oscillator when locked (video present). The leading edge of the horzontal oscillator pulse is usually set to coincide with the beginning of horizontal blanking.

The digital board has basically three sections. The horizontal timers (74123's) are driven by the horizontal oscillator pulses. They are set up so that all pulses during the horizontal blanking interval may be retimed and rephased. The vertical section is controlled by counters (74163's) and associated NAND gates and flip-flops. DIP switches A1, B1, C1, control the position of vertical blanking and drive. Switches A2, B2, C2, control the length of vertical blanking. Using A2 - C2, VB may be set anywhere from 17 to 24 horizontal lines long. Other

NAND gates on the board are used for sync recombination, and to detect when the device is locked properly to an external source.

SET UP

A dual trace oscilloscope is desirable, but not absolutely necessary. One vertical channel is connected to a high quality composite video signal (like the IP). The oscilloscope must be triggered from this source, either externally, or by channel selection. Set the scope to display several lines of video.

Follow the steps in the order given. Each step must be set up correctly before continuing to the next.

1. Using the other vertical scope channel, attach an oscilloscope probe to line B of the sync lock board. With NO VIDEO input adjust R1 so that the horizontal oscillator rate is approximately the same as that of the video.

2. With a video input at JI1, adjust R2 so that the phase of the horizontal oscillator pulse lines up with the beginning of horizontal blanking. This adjustment is a master horizontal phase control in that all pulses during the horizontal blaking interval are timed in relation to the leading edge of the horizontal oscillator pulse. When you change R2, all horizontal sync components will change phase accordingly.

3. Replace the scope probe with a 75 ohm line attached to composite blanking. Adjust RT5 for the proper length of horzontal blanking.

4. Looking at the output of horizontal drive, adjust RT6 for the proper length of HD.

5. Using the composite sync output, adjust RT3 for horizontal sync phase, and RT4 for sync length.

6. RT1 controls the phase position of burst flag, while RT2 controls its length. Burst flag is timed in relation to the leading edge of horizontal sync. Phase changes in sync will cause concurrent phase changes in burst flag.

7. Trigger the scope to display several fields of video. Using the vertical drive output, set DIP swithes A1,B1, and C1, to position VD at the beginning of the vertical blanking interval. The three switches have eight different possible position combinations. If VD is at best offset by one half line of video (advanced or delayed) from the beginning of vertical blanking, you are looking at the odd (B) field. In this case, set VD so that it is

advanced by one half line.

8. Attach the 75 ohm line to the composite blanking output. Vertical blanking should have the same phase as vertical drive. Adjust switches A2, B2, and C2, for the correct length of VB. 22 lines should be the maximum setting.

CONSTRUCTION

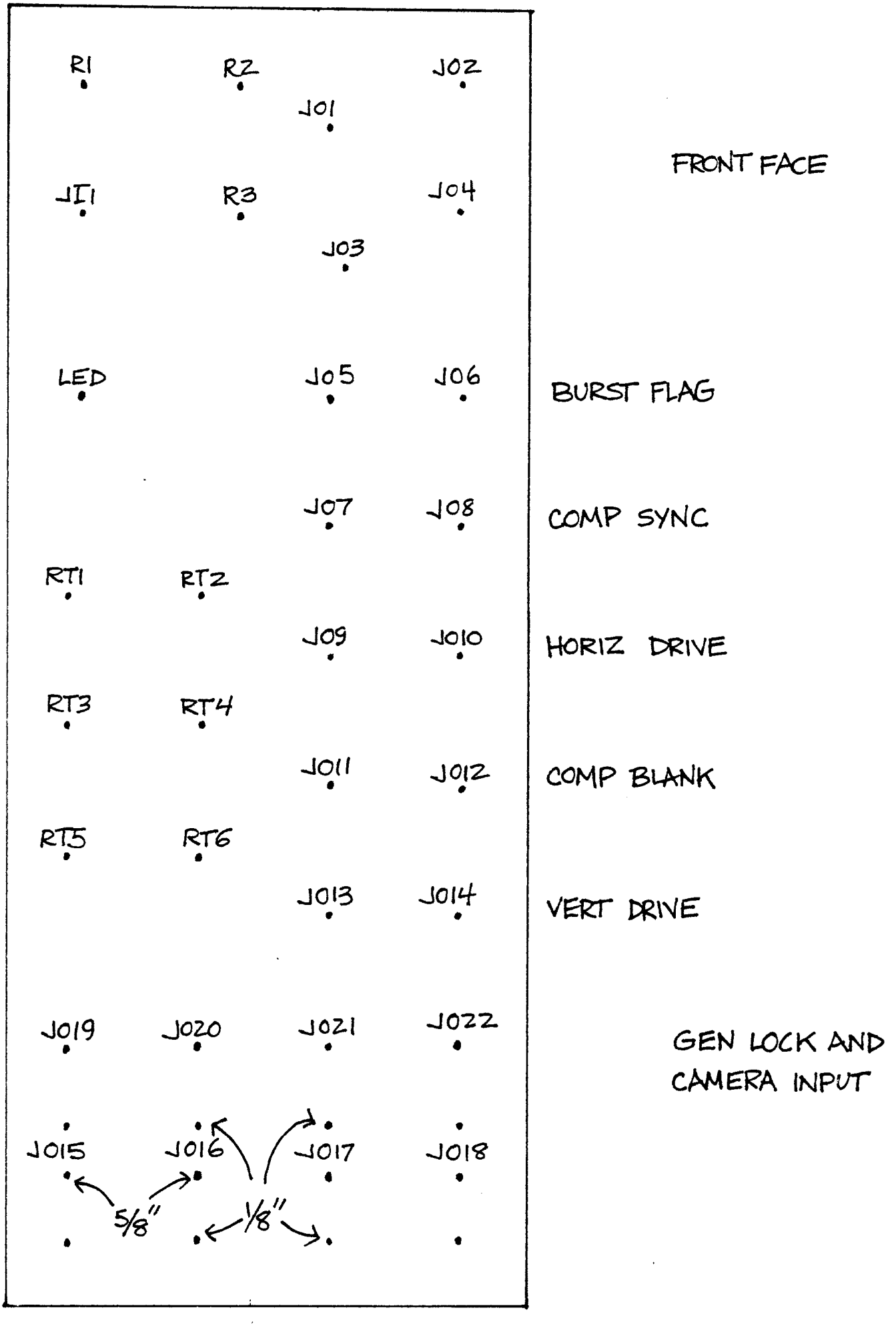
On the digital board, some wires are soldered from point to point, others are wire wrapped. Follow both the wire wrap list, and the pictorial. Remember to cut the foil, and jump ground to the outside bus, where noted.

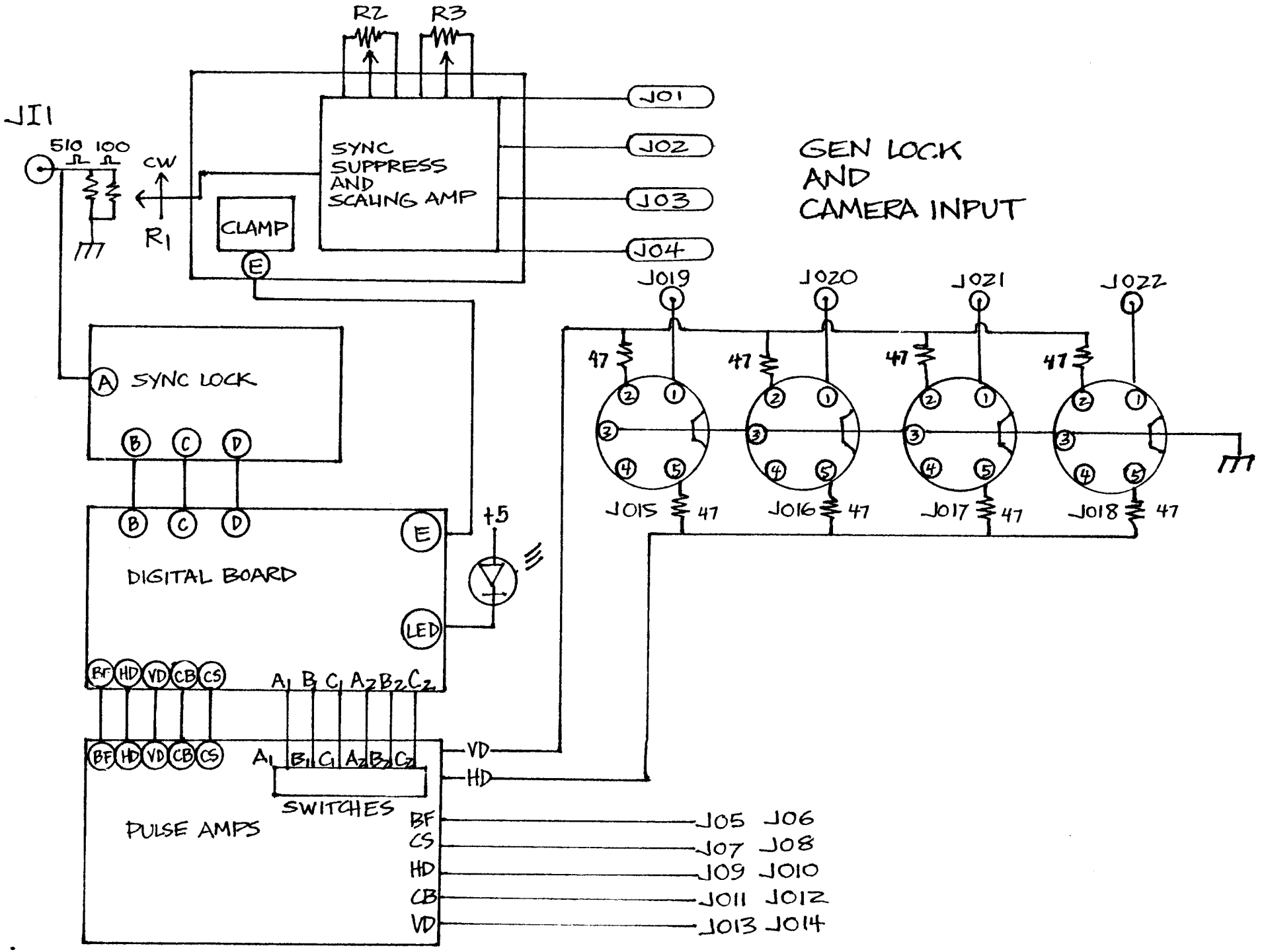
All circuit boards, except the VS5 are mounted of 1" standoff mounting posts. VS5 is mounted at the top of the module, RMGL board in the middle, and the DS6 at the bottom. Mount the digital board behind the DS6, and RMGL boards. Input/output wires on the digital board should be kept to one edge, so that the board may be swung back for replacement of IC's, troubleshooting, etc.

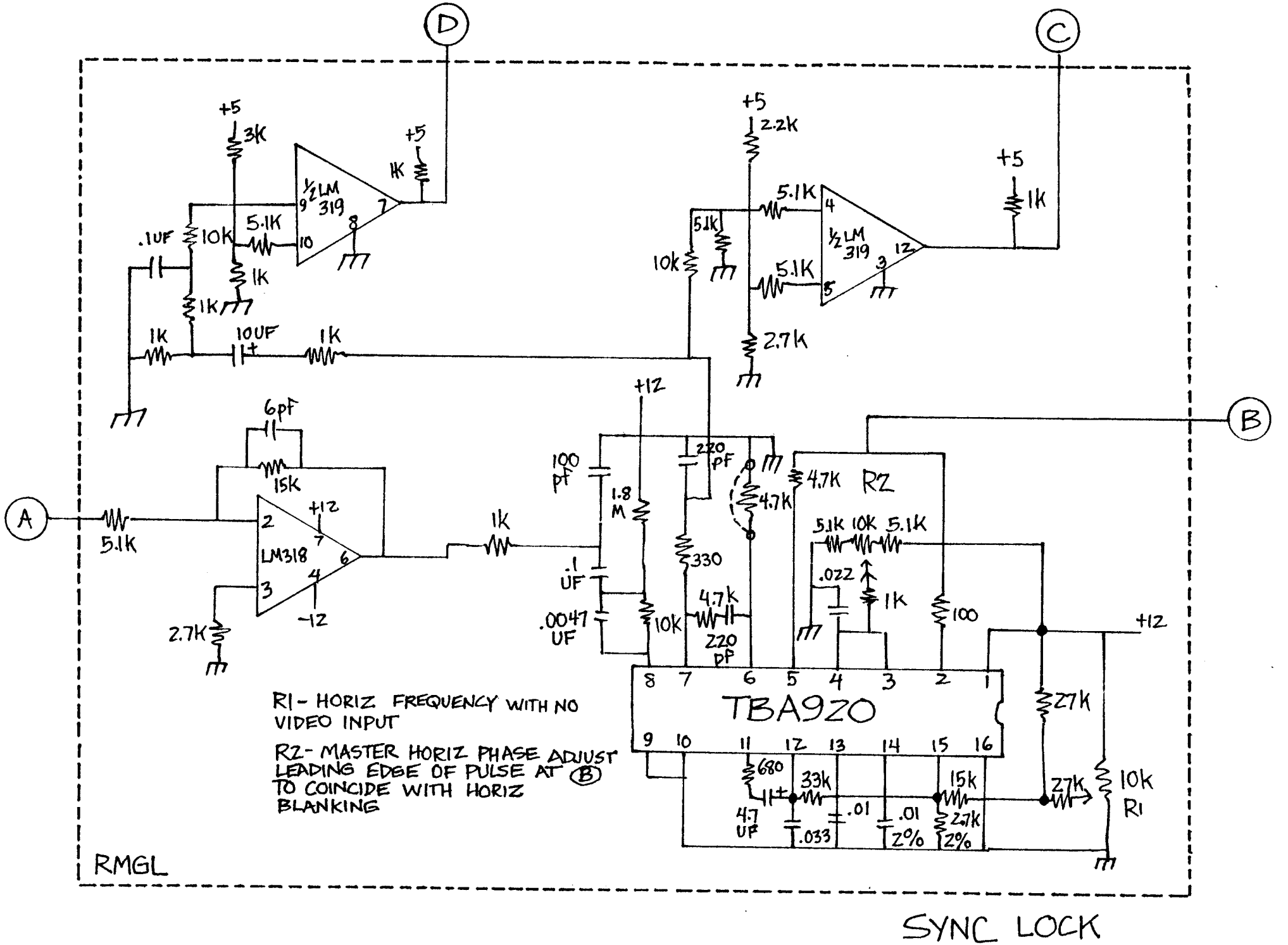
Line E from the digital board runs to point JI2 on the VS5 board. Reverse the polarity of the 10uf cap. which is in series with the 470uh choke and the 1N914 diode.

On the Pulse Amp board (DS6), mount the 7808 voltage regulator to the heat sink, and then to the board itself with a 4x40 screw.

Remember to bus ground and the appropriate power to the circuit boards. +5 volts must also be run to the front panel for the LED, and the trimmers.

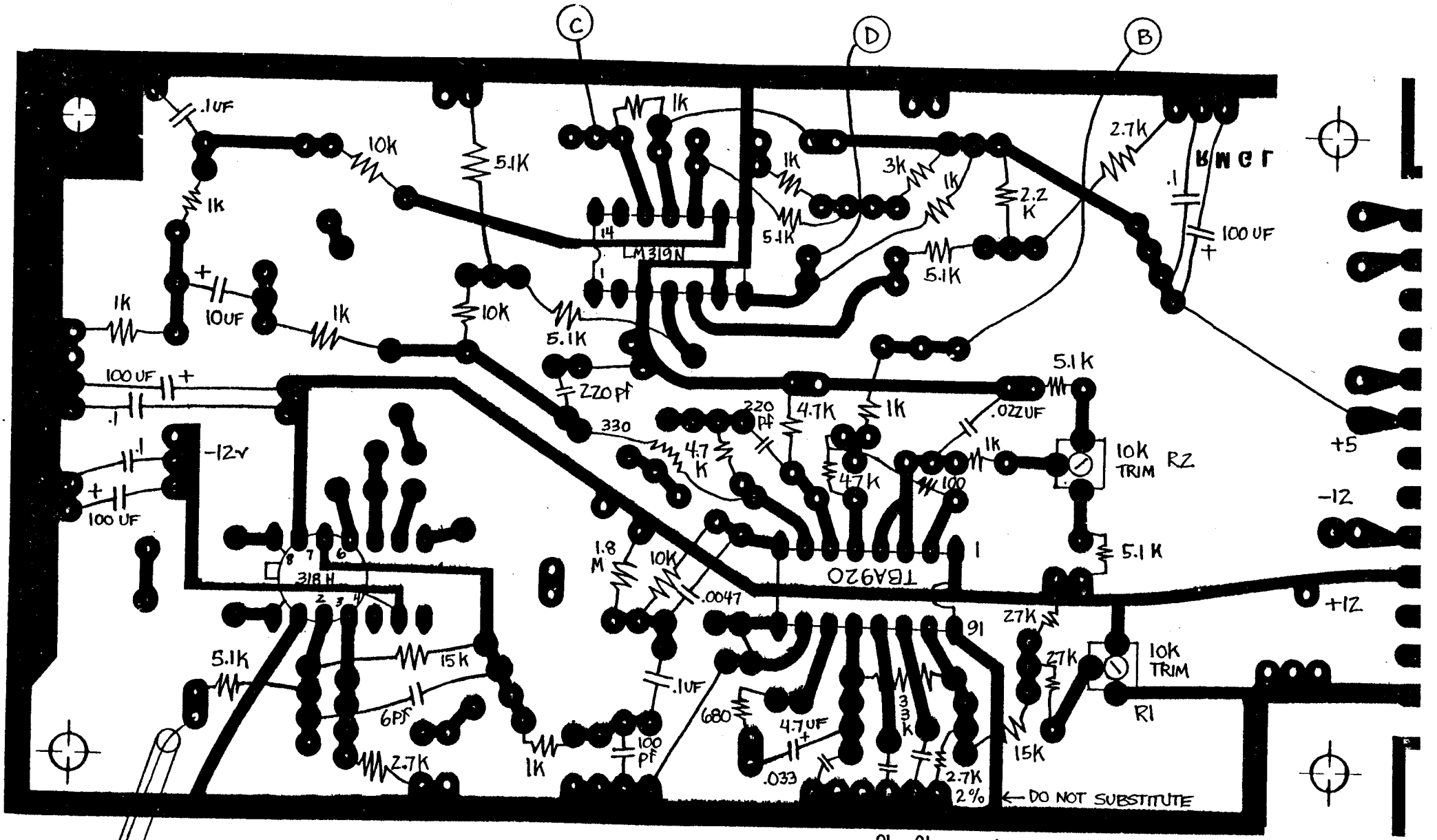

R1
R2
J02
J01
FRONT FACE
J11
R3
J04
J03
LED
J05
J06
BURST FLAG
J07
J08
COMP SYNC
RT1
RT2
J09
J010
HORIZ DRIVE
RT3
RT4
J011
J012
COMP BLANK
RT5
RT6
J013
J014
VERT DRIVE
J019
J020
J021
J022
GEN LOCK AND
CAMERA INPUT
J015
J016
J017
J018
5/8"
1/8"


R2
R3
J1
510
100
CW
R1
CLAMP
SYNC SUPPRESS AND SCALING AMP
J01
J02
J03
J04
GEN LOCK AND CAMERA INPUT
J019
J020
J021
J022
47
SYNC LOCK
A
B
C
D
E
DIGITAL BOARD
+5
LED
J015
J016
J017
J018
BF
HD
VD
CB
CS
A1 B1 C1 A2 B2 C2
SWITCHES
PULSE AMPS
J05 J06
J07 J08
J09 J010
J011 J012
J013 J014


D
C
B
A
+5
3K
1K
.1UF
10K
5.1K
1K
1K
1K
10UF
1K
½ LM 319
9
10
8
7
+5
1K
2.2K
5.1K
10K
5.1K
5.1K
2.7K
½ LM 319
4
5
12
3
+5
1K
6pF
15K
5.1K
LM318
2
3
7
6
4
+12
-12
2.7K
1K
100 pF
1.8 M
.1 UF
.0047 UF
10K
330
4.7K
220 pF
220 pF
4.7K
4.7K RZ
5.1K 10K 5.1K
.022
1K
100
+12
TBA920
8 7 6 5 4 3 2 1
9 10 11 12 13 14 15 16
680
4.7 UF
33K
.033
.01
.01
2%
15K
2.7K
2%
27K
27K
10K
RI
R1- HORIZ FREQUENCY WITH NO VIDEO INPUT
R2- MASTER HORIZ PHASE ADJUST LEADING EDGE OF PULSE AT (B) TO COINCIDE WITH HORIZ BLANKING
RMGL

SYNC LOCK

SYNC LOCK

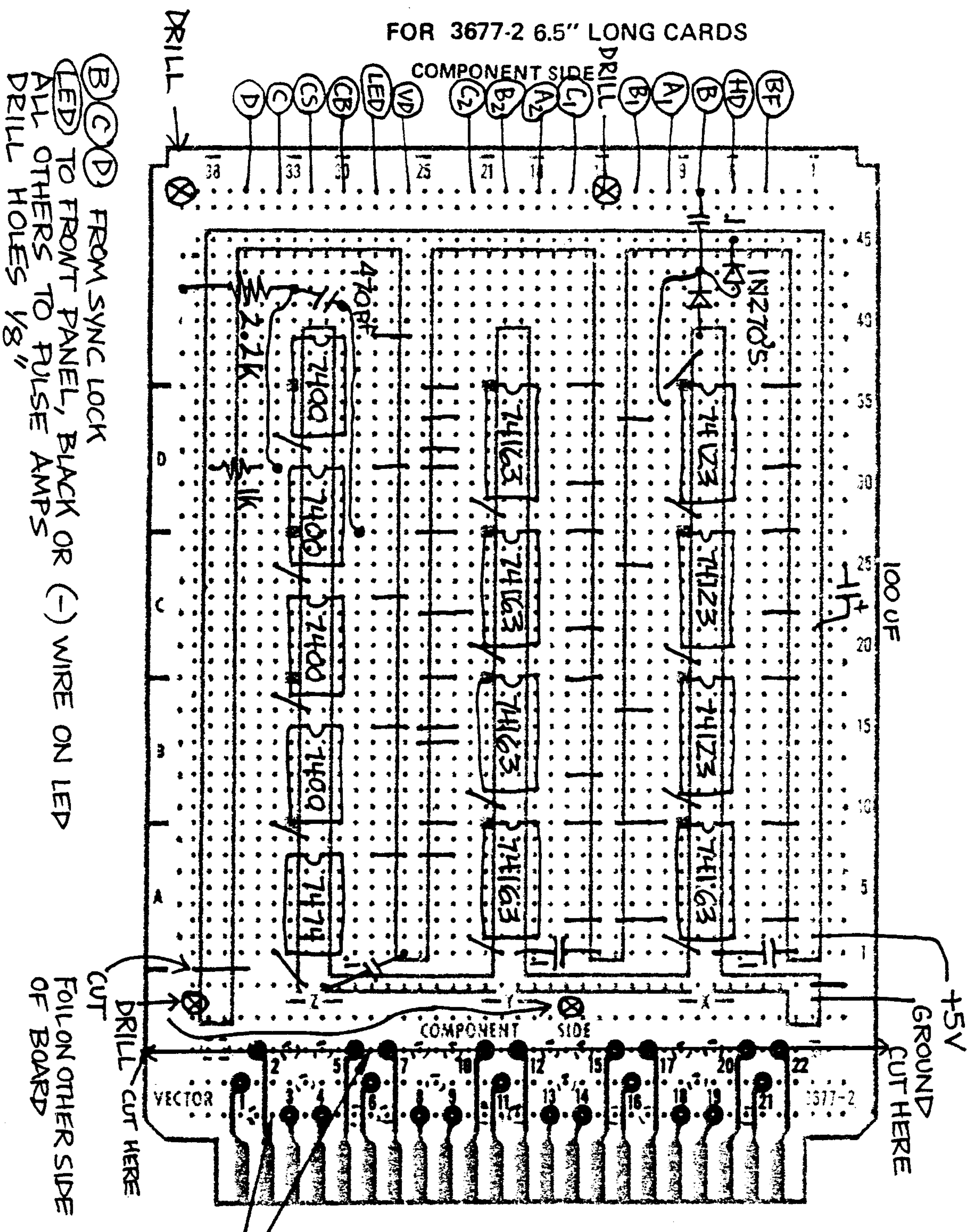


COMPONENT SIDE

CDI

DIGITAL BOARD

FOR 3677-2 6.5" LONG CARDS



CAUTION: ALL PLUG PADS ARE USABLE, BUT DO NOT USE HOLES BETWEEN PLUG PADS AND TRACES (INSUFFICIENT CLEARANCE)

NOTICE

Please disregard the very thin "skin" of solder which may appear across the opening of some holes. This is inherent in the process we use which ensures ample solder coverage of ALL circuitry. This skin is easily penetrated by even light wire component leads. A small per cent of the holes may have sufficient solder blockage to require soldering iron to open.

■ = No. 1 DIP Position

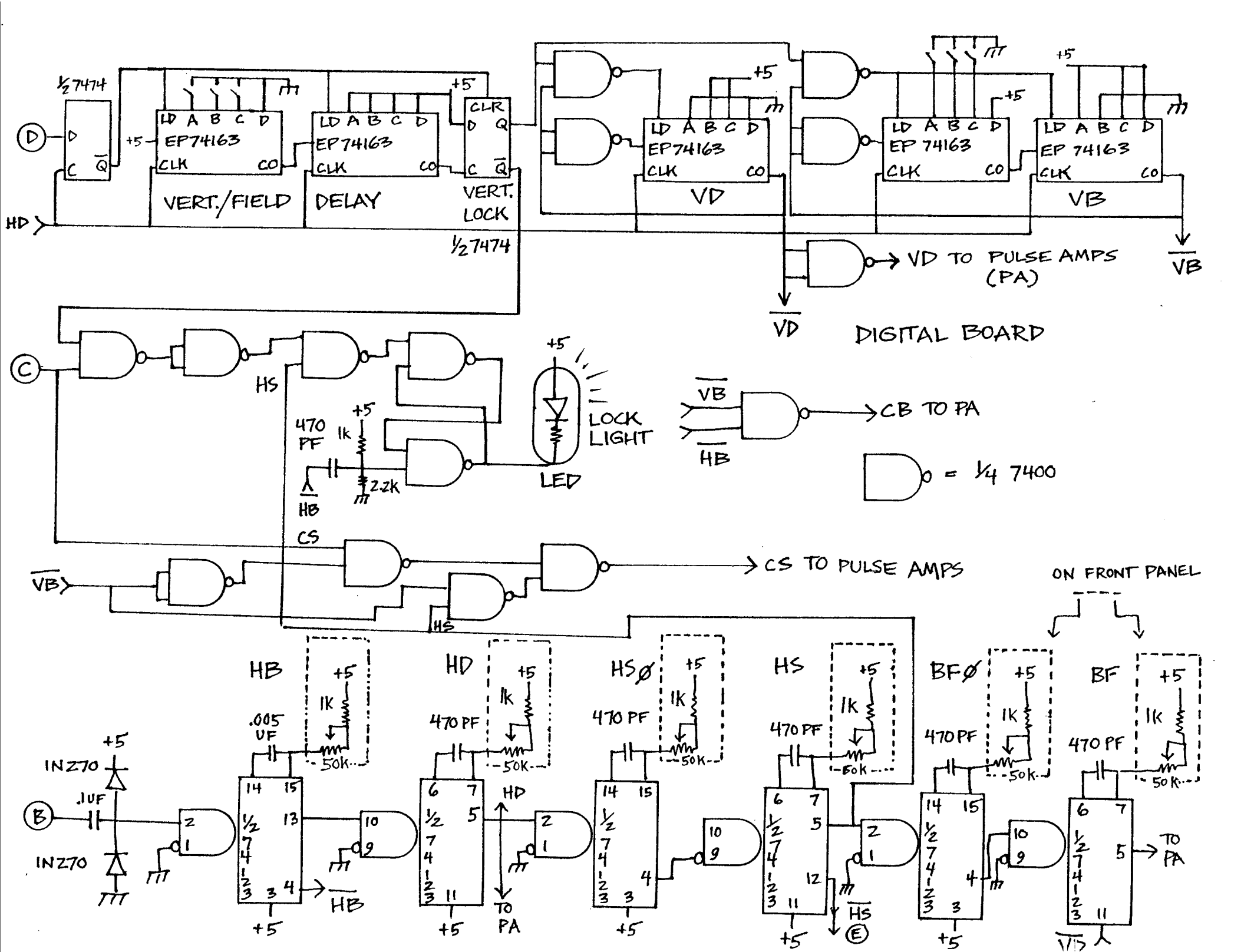
Zone Letters, A,B,C,etc., on Y axis and X,Y,Z on X axis mark position for 14- or 16-pin DIPs

NOTES

1. ZONE LETTERS A,B,C, ETC., ON Y AXIS AND X,Y,Z ON X AXIS MARK POSITION FOR 14- OR 16-PIN DIPS.
2. DOTTED CIRCLES REPRESENT PLUG PADS ON OPPOSITE SIDE OF BOARD.
3. INTENDED FOR USE IN NON-HOSTILE ENVIRONMENTS UP TO 200 VOLTS RMS OR 300 VOLTS DC.

PATTERN .042" x 0.1" SPACED HOLES
LA2-P5 LAYOUT PAPER Issue 78-1

12460 GLADSTONE AVE.
SYLMAR, CALIF. 91342


½ 7474
D
C Q
HD
LD A B C D
EP74163
CLK CO
+5
VERT./FIELD
DELAY
CLR D Q
C Q
VERT. LOCK
½ 7474
VD
VB
VD TO PULSE AMPS (PA)
DIGITAL BOARD
C
HS
470 PF
1k
2.2k
HB
LED
LOCK LIGHT
CB TO PA
= ¼ 7400
CS
CS TO PULSE AMPS
ON FRONT PANEL
HB
HD
HSØ
HS
BFØ
BF
.005 UF
50k
INZ70
.1UF
B
TO PA
TO

WIRING LIST FOR DIGITAL BOARD

IC Placement by Pin 1

IC	Pin 1 to;
74123	36,$\overline{9}$
74123	27,$\overline{9}$
74123	18,$\overline{9}$
74163	9,$\overline{9}$
74163	36,$\overline{21}$
74163	27,$\overline{21}$
74163	18,$\overline{21}$
74163	9,$\overline{21}$
7400	39,$\overline{33}$
7400	31,$\overline{33}$
7400	23,$\overline{33}$
7400	15,$\overline{33}$
7474	7,$\overline{33}$

Soldered Edge Wires

Name	Source	To
BF	47,$\overline{4}$	14,$\overline{11}$
HD	47,$\overline{6}$	32,$\overline{11}$
B	47,$\overline{8}$	see pictorial
A1	47,$\overline{10}$	7,$\overline{11}$
B1	47,$\overline{12}$	6,$\overline{11}$
C1	47,$\overline{16}$	5,$\overline{11}$
A2	47,$\overline{18}$	25,$\overline{22}$
B2	47,$\overline{20}$	24,$\overline{22}$
C2	47,$\overline{22}$	23,$\overline{22}$

Capacitors on 74123's

From	Value	To
35,$\overline{5}$	.005 uf	34,$\overline{5}$
31,$\overline{10}$	470 pf	30,$\overline{10}$
26,$\overline{5}$	470 pf	25,$\overline{5}$
22,$\overline{10}$	470 pf	21,$\overline{10}$
17,$\overline{5}$	470 pf	16,$\overline{5}$
13,$\overline{10}$	470 pf	12,$\overline{10}$

Wires to Front Panel Timmers

From	To
35,$\overline{4}$	RT5 (HB)
30,$\overline{11}$	RT6 (HD)
26,$\overline{4}$	RT3 (HS Phase)
21,$\overline{11}$	RT4 (HS)
17,$\overline{4}$	RT1 (BF Phase)
12,$\overline{11}$	RT2 (BF)
23,$\overline{5}$	E (clamp to VS5)

Soldered Edge Wires cont'd

Name	Source	To
VD	47,$\overline{26}$	10,$\overline{35}$
LED	47,$\overline{28}$	29,$\overline{35}$
CB	47,$\overline{30}$	25,$\overline{28}$
CS	47,$\overline{32}$	26,$\overline{35}$
C	47,$\overline{34}$	38,$\overline{34}$
D	47,$\overline{36}$	6,$\overline{34}$

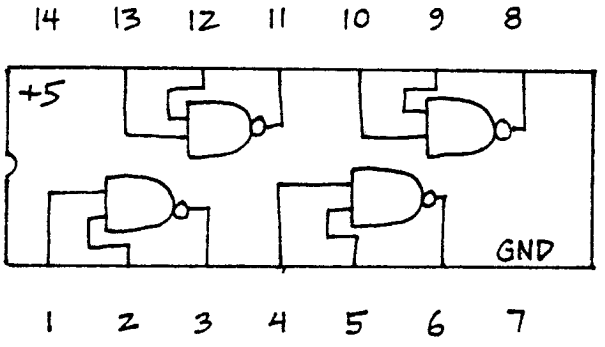
Wire Wrap List

Name	Source	To	To	To
Gnd	29,$\overline{6}$	29,$\overline{9}$	27,$\overline{9}$	
Gnd	20,$\overline{6}$	20,$\overline{9}$	18,$\overline{9}$	
Gnd	11,$\overline{6}$	11,$\overline{9}$		
HB	33,$\overline{6}$	30,$\overline{6}$		
$\overline{\text{HB}}$	33,$\overline{9}$	27,$\overline{30}$		
HD	32,$\overline{9}$	26,$\overline{9}$	8,$\overline{9}$	8,$\overline{21}$
		17,$\overline{21}$	26,$\overline{21}$	35,$\overline{21}$
		8,$\overline{21}$	5,$\overline{33}$	
$\overline{\text{HSØ}}$	24,$\overline{9}$	21,$\overline{6}$		
HS	23,$\overline{9}$	17,$\overline{9}$	23,$\overline{33}$	34,$\overline{30}$
BFØ	15,$\overline{9}$	12,$\overline{6}$		
Gnd	4,$\overline{9}$	2,$\overline{9}$		
+5	7,$\overline{21}$	6,$\overline{21}$	5,$\overline{21}$	4,$\overline{21}$
V Load	6,$\overline{30}$	2,$\overline{33}$	2,$\overline{18}$	2,$\overline{6}$
+5	7,$\overline{30}$	7,$\overline{33}$	4,$\overline{33}$	3,$\overline{30}$
Carry	8,$\overline{6}$	3,$\overline{21}$		
Carry	8,$\overline{18}$	4,$\overline{30}$		
+5	5,$\overline{30}$	7,$\overline{30}$		

Wire Wrap List con'd

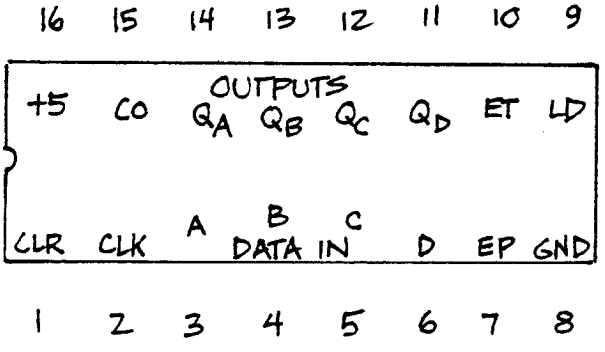
Name	Source	To	To	To
$\overline{Q}$	1,$\overline{30}$	39,$\overline{33}$		
Q	2,$\overline{30}$	10,$\overline{30}$	18,$\overline{30}$	
Carry	17,$\overline{18}$	13,$\overline{6}$		
	17,$\overline{18}$	11,$\overline{30}$	13,$\overline{30}$	14,$\overline{30}$
		12,$\overline{33}$	11,$\overline{33}$	
Load	11,$\overline{18}$	9,$\overline{30}$		
EP	12,$\overline{21}$	12,$\overline{30}$		
Gnd	16,$\overline{21}$	13,$\overline{21}$	11,$\overline{21}$	
	33,$\overline{21}$	29,$\overline{21}$		
Load	29,$\overline{18}$	20,$\overline{18}$	17,$\overline{30}$	
EP	21,$\overline{21}$	20,$\overline{30}$		
Carry	26,$\overline{18}$	30,$\overline{21}$		
Carry	35,$\overline{18}$	22,$\overline{30}$	21,$\overline{30}$	19,$\overline{30}$
		15,$\overline{33}$	14,$\overline{33}$	
	22,$\overline{30}$	22,$\overline{33}$	26,$\overline{30}$	
VBN	13,$\overline{33}$	19,$\overline{33}$		
NAND	18,$\overline{33}$	27,$\overline{33}$		
"	28,$\overline{33}$	21,$\overline{33}$		
"	23,$\overline{33}$	34,$\overline{30}$		
"	38,$\overline{33}$	20,$\overline{33}$		
"	37,$\overline{33}$	36,$\overline{33}$	35,$\overline{33}$	
"	34,$\overline{33}$	35,$\overline{30}$		
"	33,$\overline{30}$	30,$\overline{30}$		
"	29,$\overline{30}$	29,$\overline{33}$		
"	28,$\overline{30}$	31,$\overline{33}$		
+5	39,$\overline{30}$	38,$\overline{30}$	37,$\overline{30}$	

IC's ON DIGITAL BOARD

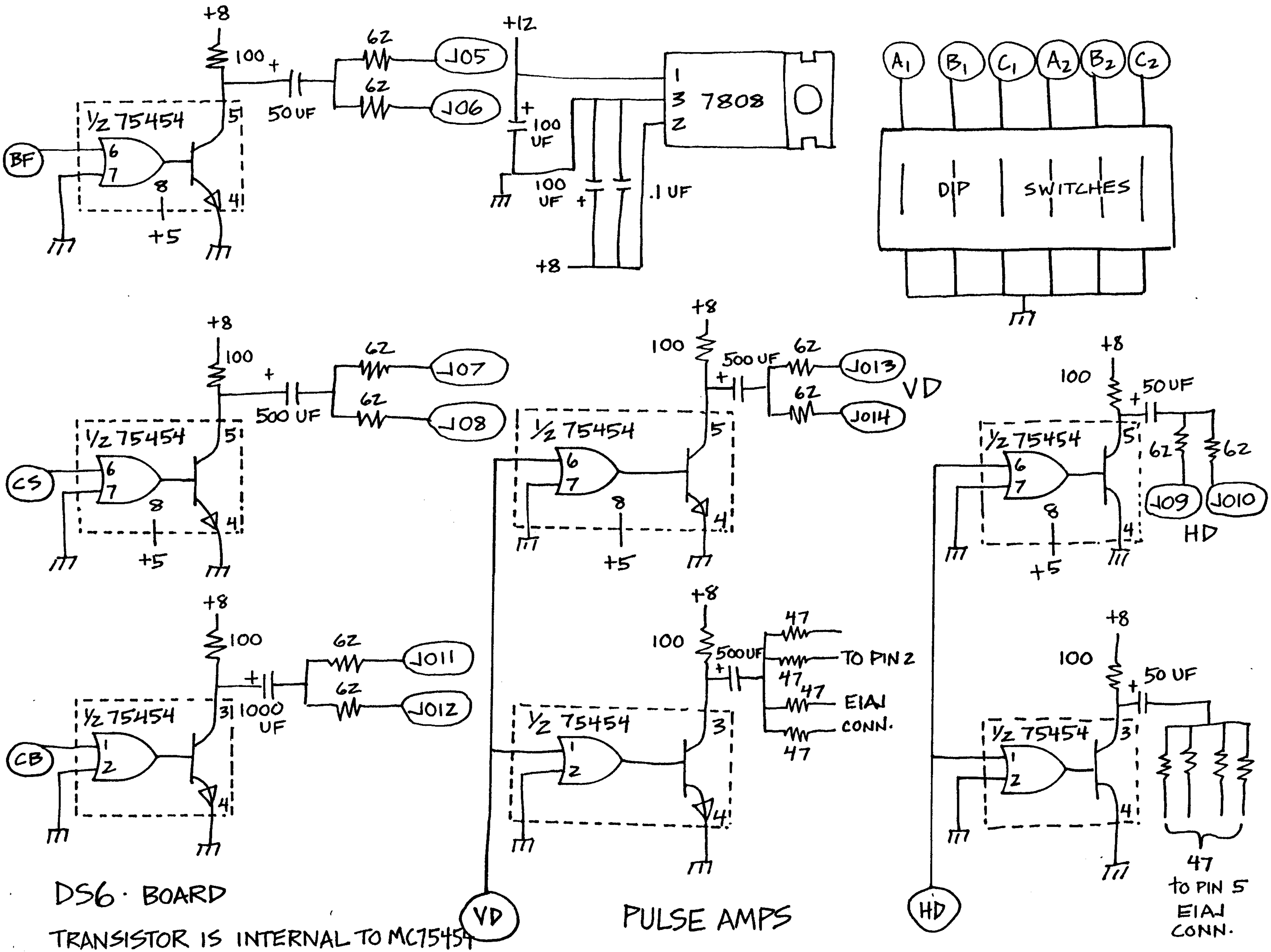


7400
QUAD NAND

7474
DUAL D TYPE FLIP FLOP

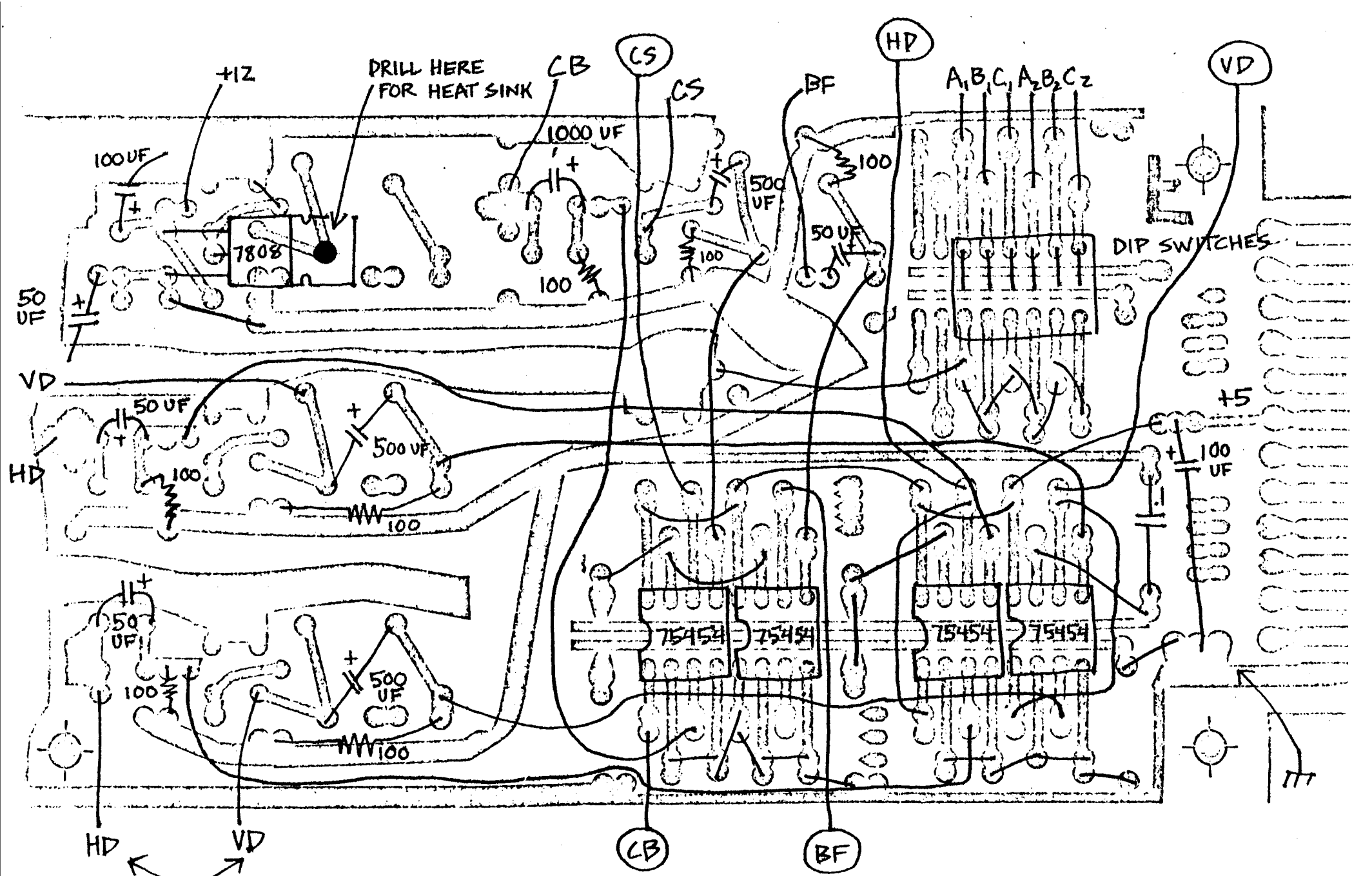


74163
4-BIT COUNTER



DS6 · BOARD

TRANSISTOR IS INTERNAL TO MC75454


+12
DRILL HERE FOR HEAT SINK
CB
CS
CS
HD
BF
A1 B1 C1 A2 B2 C2
VD
100 UF
1000 UF
500 UF
100
50 UF
7808
DIP SWITCHES
50 UF
VD
+5
HD
50 UF
500 UF
100
100
100 UF
50 UF
500 UF
100
100
75454
75454
75454
75454
HD
VD
CB
BF
TO EIA
6 PINS
USE 47Ω RESISTORS
NOTE: 62Ω RESISTORS ON FRONT PANEL
FOR PULSE OUTPUTS

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ADDENDUM TO THE GEN LOCK

In its initial design, the Gen Lock misplaces the leading edge of vertical blanking by one half line during the odd field. This circuit addition will fix that problem, and reestablish proper interlace to composite blanking. Vertical sync information is unchanged by this addition, as sync was already correctly interlaced in the previous design.

This addendum is useful to people who anticipate that much of their work will be time base corrected, or that they will be working often in a broadcast environment. The earlier design will work fine with all non-broadcast equipment, and its use does not preclude the ability to time base correct your videotapes.

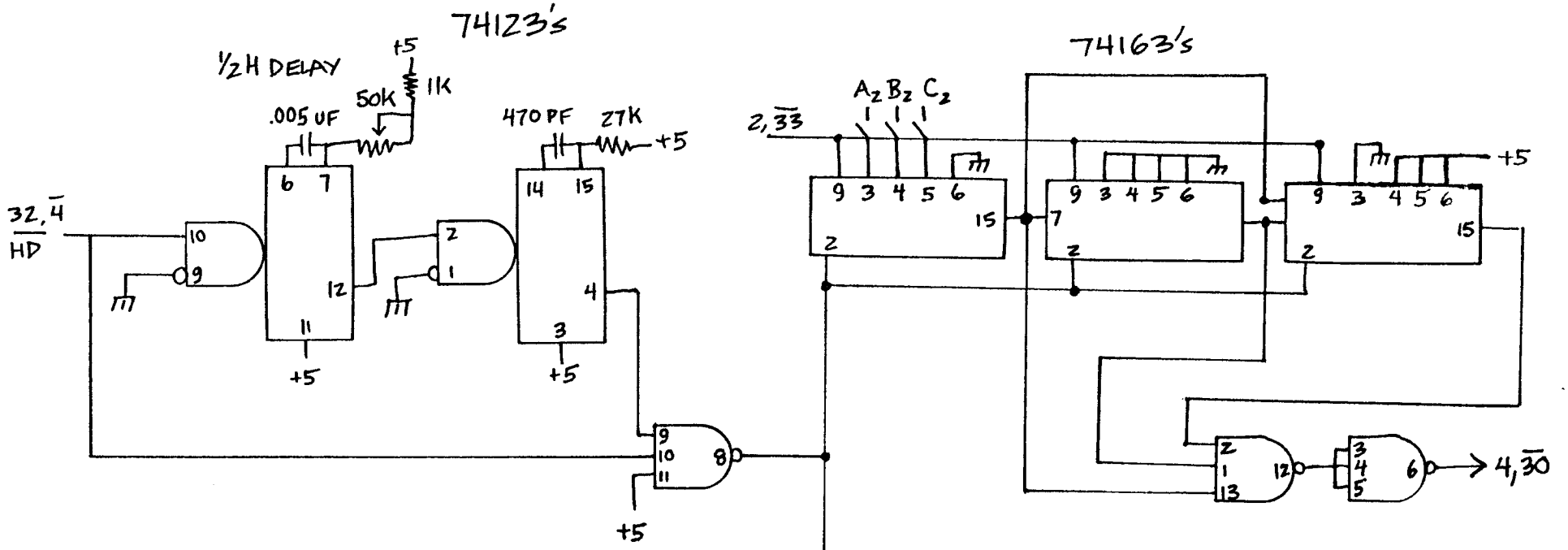
NOTE: The addition of this circuit makes the construction of the Gen Lock more complex and difficult. If you don't understand how to put it in, use the original design. The module will work fine, and you can add the additional circuit later.

CONSTRUCTION

Build the circuit on perf board, wire wrapping the connections. Mount it above the digital board. Remember to bus ground and +5 volts to the board, and bypass +5 to ground with a .1uf cap. every few IC's. Mount the 74123 and the 50k trimmer near the rear of board, with the trimmer adjust facing back. Drill a hole in the back panel in the appropriate place for the 1/2 H adjustment. On the main digital board remove the 74163 which is in line with the 74123's, and remove the 74163 below it also. Do not wire wrap wires associated with these two IC's.

SET UP

Attach an oscilloscope probe to pin 8 of the 7410. Display it, and a high quality video signal (also inputted to the Gen Lock) on both channels of the scope. Trigger the scope to show the beginning of the vertical blanking interval, including equalization pulses and sync. Adjusting the 50k trimmer will change the phase of the 1/2 line pulse. Using every other equalization pulse as a guide, adjust these pulses so that their leading edge is coincident, or slightly ahead of the leading edge of the equalization pulses.



74123 PIN 16. +5
PIN 8. m

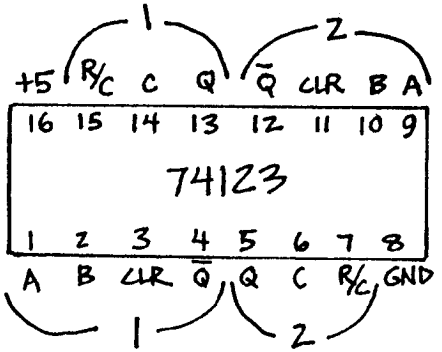
74163 PIN 16. +5
PIN 8. m
PIN 1. +5
ALL UNUSED PINS 7, 10. +5

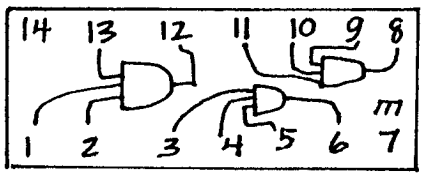
7410 PIN 14. +5
PIN 7. m

ON DIGITAL BOARD
MODIFY TO:

+5 22, $\overline{21}$, 32, $\overline{21}$,
31, $\overline{21}$

GND 34, $\overline{21}$, 33, $\overline{21}$





7410

GEN·LOCK MODIFICATION 3/79

PARTS LIST

NOTE: Only parts which are not normally used in the IP are listed. All others are standard IP parts.

Newark

1	13F148	DC-1/4 2.7k	2.74k ohm 1%
1	12F9615	3068-P-50k	50k trimmer
1	17F2202	715P10354JD3	.01uf 5%
1	38F1368	3677-2	Vector Board
1	38F1362	K32	J Pins for wire wrap
1		P184A	Vector Wire Wrap Tip
1		P185	Vector Wire Wrap Adapter
1		W28-6A	Vector Wire
1		W28-6B	" "
1		W28-6E	" "
1		W28-6F	" "
8	57F1775	C91-14-00	14 Pin Wire Wrap Socket
14	57F1776	C91-16-00	16 Pin Wire Wrap Socket
1	58F156	291-.36ABH	Heat Sink
1	57F2910	76B06	SPST 6 Rockers
1		559-0102-002	Dialight Red LED w/ internal resistor

SEMICONDUCTOR SPECIALISTS OR HAMILTON AVNET

1	TBA920	Horizontal Oscillator	Fairchild
1	uA7808UC	+8 Volt Regulator	Fairchild
1	LM319N	Comparator	National
4	MC75454P	Peripheral Driver	Motorola
1	LM318H	Op Amp	National
2	CA3030	Op Amp	RCA
4	DM74123N	Mono Multi	National
6	DM74163AN	4 Bit Counter	"
1	DM7474N	Flip Flop	"
1	DM7410N	Triple In NAND	"
4	DM7400N	Quad NAND	"

ECI

1	VS5
1	DS6
1	RMGL